What is claimed is:

1. A method of forming post passivation interconnects for an integrated circuit having a plurality of contact regions, the method comprising:

forming a passivation layer over the integrated circuit, the passivation layer, formed from a non-oxide material;

forming a buffer layer over the passivation layer, the buffer layer comprising a silicon oxide layer with a thickness substantially smaller than a thickness of the passivation layer;

removing a top portion of the buffer layer;

depositing a post passivation metal layer over the buffer layer after removing a top portion of the buffer layer; and

forming a connection pattern in the post passivation metal layer such that portions of the connection pattern are electrically coupled to the contact regions.

2. The method of claim 1 wherein the top portion of the buffer layer is removed in a cleaning chamber having an inner wall comprising primarily quartz.

3. The method of claim 2 wherein the cleaning chamber is in a vacuum condition during the removing step and wherein the post passivation metal layer is deposited over the buffer layer after the removing step without breaking the vacuum condition in the cleaning chamber.

4. The method of claim 1 wherein passivation layer is formed in a first chamber that is in a vacuum condition and wherein the buffer layer is formed over the passivation layer

in the first chamber and without breaking the vacuum condition in the first chamber after forming the passivation layer.

5. The method of claim 4 wherein the top portion of the buffer layer is removed in the first chamber, the method further comprising breaking a vacuum condition in the first chamber before the step of etching the buffer layer.

6. The method of claim 1 wherein the passivation layer comprises a layer of silicon nitride.

7. The method of claim 1 wherein the passivation layer comprises more than one layer and wherein an uppermost layer comprises silicon nitride.

8. The method of claim 1 wherein the buffer layer has a thickness less than about 25 nanometers.

9. The method of claim 1 wherein the ratio of the thickness of the passivation layer to the thickness of the buffer layer is greater than about 20.

10. A method of depositing a conductive layer over an integrated circuit, the method comprising:

providing a substantially completed integrated circuit, the substantially completed integrated circuit including a silicon nitride passivation layer at an uppermost surface;

forming an oxide buffer layer over and abutting the silicon nitride passivation layer, the oxide buffer layer having a thickness substantially smaller than a thickness of the passivation layer;

forming a metal layer over and abutting the oxide buffer layer; and

patterning the metal layer.

11. The method of claim 10 wherein the oxide buffer layer is etched in a chamber that includes quartz inner walls.

12. The method of claim 10 wherein the thickness of the silicon nitride passivation layer is at least about 20 times greater than the thickness of the oxide buffer layer.

13. The method of claim 12 wherein the oxide buffer layer has a thickness of less than about 25 nm.

14. A semiconductor device comprising:

a silicon substrate having a plurality of active devices formed therein, the active devices being interconnected by a plurality of metal layers including an uppermost metal layer, the uppermost metal layer including a plurality of contact regions;

a nitride passivation layer overlying the uppermost metal layer except for a portion of the contact regions;

an oxide buffer layer overlying the passivation layer, the buffer layer having a thickness substantially smaller than a thickness of the passivation layer; and

a post passivation metal layer overlying the oxide buffer layer, the post passivation metal layer patterned so as to electrically couple the plurality of contact regions to a plurality of contact pads formed in the post passivation metal layer.

15. The semiconductor device of claim 14 wherein the nitride passivation layer is formed from silicon nitride and the oxide buffer layer is formed from silicon oxide.

16. The semiconductor device of claim 14 wherein the thickness of the oxide buffer layer is less than 25 nanometers.

17. The semiconductor device of claim 14 wherein thickness of the nitride passivation layer is at least about 20 time greater than the thickness of the oxide buffer layer.

18. A packaged integrated circuit comprising:

a semiconductor chip having a plurality of active devices formed therein, the active devices being interconnected by a plurality of metal layers including an uppermost metal layer, the uppermost metal layer including a plurality of contact regions disposed around the periphery of the chip;

a nitride passivation layer overlying the uppermost metal layer except for a portion of the contact regions;

an oxide buffer layer overlying the passivation layer, the buffer layer having a thickness substantially smaller than a thickness of the passivation layer;

a post passivation metal layer overlying the oxide buffer layer, the post passivation metal layer patterned so as to electrically couple the plurality of contact regions to a plurality of contact pads formed in the post passivation metal layer, the contact pads being arranged over a central portion of the semiconductor chip;

a package substrate having a plurality of contact pads arranged in a configuration corresponding to the contact pads on the semiconductor chip; and

a plurality of solder bumps disposed between the semiconductor chip and the package substrate so as to electrically couple the contact pads on the semiconductor chip with the contact pads on the package substrate.

19. The packaged integrated circuit of claim 18 wherein the semiconductor chip comprises a logic device.

20. The packaged integrated circuit of claim 19 wherein the uppermost metal layer comprises a layer of copper.

21. The packaged integrated circuit of claim 20 wherein thickness of the nitride passivation layer is at least about 20 time greater than the thickness of the oxide buffer layer.